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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,038	05/30/2006	Katsumasa Hijikata	064766-0015	6906
53080	7590	02/18/2009	EXAMINER	
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096				TRAN, PABLO N
ART UNIT		PAPER NUMBER		
2618				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,038	HIJIKATA ET AL.	
	Examiner	Art Unit	
	Pablo N. Tran	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 November 2008.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.
 4a) Of the above claim(s) 2,4,6,8-13,18,20 and 22 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,5,14-17,19 and 21 is/are rejected.
 7) Claim(s) 3 and 7 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II (claims 1, 3, 5, 7, 14-17, 19, and 21) in the reply filed on 11/20/08 is acknowledged.
2. Claims 2, 4, 6, 8-13, and 18, 20, and 22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Groups I, III, IV, V, VI, VII, VIII there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/20/08.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 14-15, 17, and 19, rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Regarding claims 14 and 17, recites the limitation, "the first to fourth bypass current sources", render the claims indefinite.
6. Regarding claim 15, recites the limitation, "the single balance mixer, and the double balance mixer", render the claims indefinite.

7. Regarding claim 19, recites the limitation, “the double balance mixer”, render the claims indefinite.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1 and 14-16 rejected under 35 U.S.C. 102(e) as being anticipated by Igarashi et al. (hereinafter “Igarashi”, JP No 04129407).

As per claim 1, Igarashi disclose a mixer circuit including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a power supply and a ground; an RF signal supplier for supplying an RF signal to the RF signal processing portion; an LO signal supplier for supplying an LO signal to the LO signal processing portion; and at

least a bypass current supply portion for bypassing a bias current of the LO signal processing portion (see fig. 1-3).

As per claims 14, Igarashi disclose bias circuit having a bias voltage output terminal, and a current source transistor having a gate terminal connected to the bias voltage output terminal (see fig. 1-3).

As per claims 15, Igarashi disclose MOS transistor (see fig. 1-3).

As per claims 16, Igarashi disclose the mixer circuit is one which is employed in a receiving system according to a direct conversion system, or a receiving system according to a Low IF system (see fig. 1-3).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5, 17, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Igarashi et al. (hereinafter “Igarashi”, JP No 04129407) in view of Tanaka (JP No 09069730).

As per claim 5, Igarashi disclose a mixer circuit including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a supply voltage and a ground; an RF signal supplier for supplying an RF signal to the RF signal processing portion; an LO

signal supplier for supplying an LO signal to the LO signal processing portion; at least one bypass current supply portion for bypassing a bias current of the LO signal processing portion; and said IF signal output load portion including a first load resistor having an end connected to the power supply and another end connected to a first IF output terminal, and a second load resistor having an end connected to the power supply and another end connected to a second IF output terminal; the RF signal processing portion including an RF transistor having a source terminal connected to the ground; said LO signal processing portion including a first LO transistor having a source terminal connected to a drain terminal of the RF transistor and a drain terminal connected to the first IF output terminal, and a second LO transistor having a source terminal connected to the drain terminal of the RF transistor and a drain terminal connected to the second IF output terminal (see fig. 1-3).

Igarashi is silent about a single balance mixer. However, Tanaka disclose a double (two single balance mixers connected in parallel) and a single balance mixer (see fig. 1 & 2, wherein the double balance mixer, as disclosed in Igarashi, has similar structure of two single balance mixer connected in parallel. Also see search report, page 5). Therefore, it would have been obvious to one of ordinary skill in the art for Igarashi to utilize such teaching in order to minimize offset voltages.

As per claims 17, Igarashi disclose bias circuit having a bias voltage output terminal, and a current source transistor having a gate terminal connected to the bias voltage output terminal (see fig. 1-3).

As per claims 19, Igarashi disclose MOS transistor (see fig. 1-3).

As per claims 21, Igarashi disclose the mixer circuit is one which is employed in a receiving system according to a direct conversion system, or a receiving system according to a Low IF system (see fig. 1-3).

Allowable Subject Matter

12. Claims 3 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pablo Tran whose telephone number is (571)272-7898. The examiner normal hours are 9:30 -5:00 (Monday-Friday). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban, can be reached at (571)272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) System. Status information for Published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should You have questions on access to the Private PAIR system, contact the Electronic

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in USA or CANADA) or 571-272-1000.

February 16, 2009

/Pablo N Tran/
Primary Examiner, Art Unit 2618